REMARKS

After the present amendment, claims 1-65 remain pending in the present application. Claims 60-65 have been added by way of the present amendment. Claims 1, 2, 8, 16, 22, 29, 31, 33, 37, 42, 45-46, 51, and 57 have been amended. Reconsideration and allowance of outstanding claims 1-65 in view of the amendments and following remarks is requested.

A. Rejection of Claims 1-4, 8-10, 12-13, 15-18, 22-24, 26-27, 29-40, 45-48, and 50-59 under 35 USC §102(e)

The Examiner has rejected claims 1-4, 8-10, 12-13, 15-18, 22-24, 26-27, 29-40, 45-48, and 50-59 under 35 USC §102(e) as being anticipated by U.S. Patent Application Number 6,396,539 B1 to Heller, et al. ("Heller"). For the reasons discussed below, Applicant respectfully submits that the present invention, as defined by amended independent claims 1, 29, 37, 45, 51, and 57, is patentably distinguishable over Heller.

As explained in the present application, there is a need in the art for an improved process and system for storing addresses of defective pixels in an imaging device for later retrieval. The present invention relates to a permanently programmable solid-state device, in one embodiment.

In accordance with one embodiment disclosed in the present application at page 9, lines 11-22, one time programmable ("OTP") device 100 includes:

> "a driver circuit 104 that drives the programmable memory unit 102. The driver circuit 104 includes a number of logic inverters that drive the terminals of the MOSFETs in the programmable memory unit 102, and a number of high-voltage drivers (e.g., amplifiers) that drive the gates of the MOSFETs in the programmable memory unit 102. When the programmable memory unit 102 is encoded, the drivers drive the voltage levels into the MOSFETs to predetermined values based on whether a logic state 1 or logic state 0 is to be represented in the MOSFET.

The OTP device 100 further includes access circuit 106. The access circuit 106 has a number of amplifiers that output a logic state 1 or logic state 0 from a given MOSFET corresponding to the state of breakdown or intactness of the gate oxide of that MOSFET."

Driver circuit 104 is separate from access circuit 106 as described herein and as shown in Figures 1 and 5. Moreover, driver circuit 104 and access circuit 106 fulfill different functions from each other. Driver circuit 104 is used for writing to programmable memory unit 102. Driver circuit 104 programs the programmable memory unit with addresses of defective pixels by programming memory cells within the programmable memory unit with a first logic value or a second logic value. The first logic value represents a good (i.e. non-defective) pixel at the corresponding location (e.g. address). The second logic value represents a defective pixel at the corresponding location. The individual memory cells are associated with respective pixel locations. Referring to Figure 8 and the corresponding written description, driver circuit 104 is configured to drive an inverter to ground corresponding to a row of the memory cells that are to be programmed.

Access circuit 106 is used for accessing programmable memory unit 102 and is used for identifying addresses of defective pixels. Referring to Figure 8 and the corresponding written description, access circuit 106 is configured to drive a row of the memory cells to ground that are to be read out.

In order to further define the invention and its differences and advantages, Applicant has amended independent claims 1, 29, 37, 45, 51, and 57 to recite various features related driver circuit 104 and/or access circuit 106 as discussed herein. Further, new claims 60-65 have been added that further describe the operation of access circuit 106 as discussed herein.

In contrast to the present invention, Heller discloses single controller unit 16 including analog-to-digital circuitry. See, for example, Heller at column 3, line 57 and Figure 2. In Heller, the operation of system 100 is orchestrated by system controller 122. System controller 122 is connected to communication interface 124. See, for example, Figure 1 of Heller. Heller does not teach driver circuit 104 for writing to programmable memory unit 102, and separate access circuit 106 for accessing programmable memory unit 102 and for identifying addresses of defective pixels.

Further, Heller does not teach other aspects of the present invention as discussed above and as recited in the amended independent claims. For example, Heller does not teach an access circuit configured to drive a row of the memory cells to ground that are to be read out. Therefore, Heller does not disclose, teach, or suggest the present invention as defined by amended independent claims 1, 29, 37, 45, 51, and 57.

For the foregoing reasons, Applicant respectfully submits that the present invention as defined by amended independent claims 1, 29, 37, 45, 51, and 57 is not taught, disclosed, or suggested by Heller. Thus, amended independent claims 1, 29, 37, 45, 51, and 57 are patentably distinguishable over Heller. As such, the claims depending from amended independent claims 1, 29, 37, 45, 51, and 57 are, *a fortiori*, also patentably distinguishable over Heller for at least the reasons presented above and also for additional limitations contained in each dependent claim.

B.   <u>Rejection of Claims 5-7, 11, 14, 19-21, 25, 28, 41-44, 49 under 35 USC §103(a)</u>

The Examiner has rejected claims 11, 25, and 49 under 35 USC §103(a) as being obvious with respect to Heller in view of U.S. Patent Number 6,141,453 to Banham, et al. ("Banham"). The Examiner has rejected claims 5-7 and 19-21 under 35 USC §103(a) as being obvious with

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respect to Heller in view of U.S. Patent Application Number US 2002/0001219 A1 to Forbes, et al. ("Forbes"). The Examiner has rejected claims 14, 28, and 41-42 under 35 USC §103(a) as being obvious with respect to Heller in view of U.S. Patent Number 6,532,514 B1 to Haroun, et al. ("Haroun"). The Examiner has rejected claims 43-44 under 35 USC §103(a) as being obvious with respect to the combination of Heller, Haroun, and U.S. Patent Number 5,410,511 to Michiyama ("Michiyama").
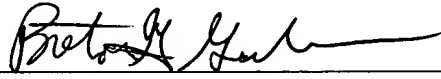
Applicant respectfully submits that claims 5-7, 11, 14, 19-21, 25, 28, 41-44, and 49 depend from amended independent claims 1, 29, 37, 45, 51, and 57, and thus, claims 5-7, 11, 14, 19-21, 25, 28, 41-44, and 49 should be allowed at least for the same reasons discussed above in conjunction with patentability of the amended independent claims.

C.   Conclusion

Based on the foregoing reasons, the present invention, as defined by amended independent claims 1, 29, 37, 45, 51, and 57, and claims depending therefrom, is patentably distinguishable over the art cited by the Examiner. Thus, outstanding claims 1-59 pending in the present application are patentably distinguishable over the art cited by the Examiner. As such, and for all the foregoing reasons, an early allowance of outstanding claims 1-59 and an early Notice of Allowance directed to all claims 1-65 remaining in the present application are respectfully requested.

Respectfully Submitted,
FARJAMI & FARJAMI LLP

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Breton G. Graham
Reg. No. 48,149

FARJAMI & FARJAMI LLP
26522 La Alameda Ave., Suite 360
Mission Viejo, California 92691
Telephone: (949) 282-1000
Facsimile: (949) 282-1002

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